

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information			
معلومات المادة الدراسية			
Module Title	Digital Logic Design I		Module Delivery
Module Type	Core		☒ Theory ☐ Lecture ☒ Lab ☐ Tutorial ☐ Practical ☒ Seminar
Module Code	MECT 106		
ECTS Credits	6.00		
SWL (hr/sem)	150		
Module Level		Semester of Delivery	
Administering Department	Mechatronics	College	Technical Engineering college
Module Leader	Hussein F. Hamdan	e-mail	eng.hussain.fadhle@uobabylon.edu.iq
Module Leader's Acad. Title	Prof.	Module Leader's Qualification	Ph.D.
Module Tutor	None	e-mail	
Peer Reviewer Name	Hussein F. Hamdan	e-mail	eng.hussain.fadhle@uobabylon.edu.iq
Scientific Committee Approval Date		Version Number	1.0

Relation with other Modules			
العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	Semester	
Co-requisites module	None	Semester	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims	1. To teach various number systems, binary codes and their applications 2. To familiarize the students the importance of error detection and error correction codes. 3. To inculcate concepts of K-MAP to simplify a Boolean expression 4. To facilitate students in designing a logic gate circuit.
Module Learning Outcomes	Upon completion of the course, students should be able to: 1. Use number systems and complements 2. Identify the importance of minimization of Boolean formulas in general and digital circuits. 3. Minimize functions using any type of minimizing algorithms. 4. Student should be able to analyze Digital Circuits using Boolean Algebra, K-maps, and Binary Number systems. 5. Analyze the design procedures of logic gate circuits.
Indicative Contents	Indicative content includes the following. 1. Binary Systems – Five Lectures ○ Introduction ○ Number Systems and Conversions ○ Arithmetic with number systems ○ Signed and unsigned number systems and their arithmetic ○ Binary Codes 2. Boolean Algebra & Logic Gates – Five Lectures ○ Boolean Postulates & Theorems ○ Boolean Functions and their Complements ○ Sum of Product Terms & Product of Sum Terms ○ Standard forms & Canonical Forms ○ Digital logic gates 3. Gate level Minimization – Five Lectures ○ Karnaugh maps ○ Multi-variable (2,3,4,5) K-maps ○ Don't care conditions ○ Digital Circuits using Basic and Universal Gates

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	Assessment is based on hand-in assignments, written exam, Case study, Quizzes, seminars, Practical testing and Online testing.

Student Workload (SWL) الحمل الدراسي للطلاب			
Structured SWL (h/sem)		Structured SWL (h/w)	
Unstructured SWL (h/sem)		Unstructured SWL (h/w)	
Total SWL (h/sem)			

Module Evaluation تقييم المادة الدراسية					
		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	4	20% (20)		
	Assignments	2	10% (10)		
	Seminar	1	10% (10)		
Summative assessment	Midterm Exam	2 hr	10% (10)		
	Final Exam	3hr	50% (50)		
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري محتوى كل اسبوع يجب ان يغطي الوقت المحدد	
	Material Covered
Week 1	Introduction
Week 2	Number Systems and Conversions
Week 3	Arithmetic with number systems
Week 4	Signed and unsigned number systems and their arithmetic
Week 5	Binary Codes
Week 6	Boolean Postulates & Theorems
Week 7	Boolean Functions and their Complements

Week 8	Sum of Product Terms & Product of Sum Terms
Week 9	Standard forms & Canonical Forms
Week 10	Digital logic gates
Week 11	MID EXAM
Week 12	Karnaugh maps
Week 13	Multi-variable (2,3,4,5) K-maps
Week 14	Don't care conditions
Week 15	Digital Circuits using Basic and Universal Gates

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Instructions to Logic design Lab, devices, groups, report preparing
Week 2	Introduction to logic gates and different digital ICs
Week 3	NOT, AND, OR Gates
Week 4	NAND, NOR Gates
Week 5	XOR gate
Week 6	Exam 1
Week 7	Truth tables and simplification using Boolean algebra
Week 8	Truth tables and K-maps
Week 9	Construction of adders, subtractors, magnitude comparators using basic gates
Week 10	Construction of BCD adder and Adder/Subtractor circuit Objective
Week 11	Exam 2
Week 12	Multiplexers
Week 13	Decoders
Week 14	Preparing to Final Exam
Week 15	Final EXAM

Learning and Teaching Resources		
مصادر التعلم والتدريس		
	Text	Available in the Library?
Recommended Texts	➤ Recommended Text Books: Mano, M Morris; Digital Design 5th Ed, Dorling Kindsley Pearson Education, 2016, ISBN: 9789332535763	
Reference Books:	➤ Digital Systems; Principles and Applications. Tocci, Widmer & Moss. 10th Edition ➤ Jain, R.P.; Logic Design ➤ Digital Principles, 3rd Ed, Roger L Tokheim; Shaum's Outlines Series	

Grading Scheme				
مخطط الدرجات				
Group	Grade	التقدير	Marks (%)	Definition
Success Group (50 - 100)	A - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 - 49)	FX - Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F - Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.

أ.د. هارون عبد الكاظم شهد
العميد

عميد الكلية : أ.د. هارون عبد الكاظم شهد
التاريخ : 2026 / 3 / 24

HF Hamdan

رئيس القسم : أ.د. حسين فاضل حمدان
التاريخ : 2026 / 3 / 24

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اسم التدريسي: أ.د. حسين فاضل حمدان
التاريخ : 2026 / 3 / 24