

UNIVERSITY OF Hilla		LECTURE : 3
ENGINEERING FACULTY		SUBJECT : power Electronics
Medical Device Technology Engineering		LECTURE'S TITLE: SCR Triggering cct.s
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SCR Firing Circuits

There are various triggering methods to turn the SCR, gate triggering is the most efficient and reliable method. Most of the control applications use this type of triggering because the desired instant of SCR turning is possible with gate triggering method. Let us look on various firing circuits of SCR.

1- Resistance Firing Circuit

The circuit below shows the resistance triggering of SCR where it is employed to drive the load from the input AC supply. Resistance and diode combination circuit acts as a gate control circuitry to switch the SCR in the desired condition.

As the positive voltage applied, the SCR is forward biased and doesn't conduct until its gate current is more than minimum gate current of the SCR.

When the gate current is applied by varying the resistance R_2 such that the gate current should be more than the minimum value of gate current, the SCR is turned ON. And hence the load current starts flowing through the SCR.

The SCR remains ON until the anode current is equal to the holding current of the SCR. And it will switch OFF when the voltage applied is zero. So the load current is zero as the SCR acts as open switch.

The diode protects the gate drive circuit from reverse gate voltage during the negative half cycle of the input. And Resistance R_1 limits the current flowing through the gate terminal and its value is such that the gate current should not exceed the maximum gate current.

It is the simplest and economical type of triggering but limited for few applications due to its disadvantages.

In this, the triggering angle is limited to 90 degrees only. Because the applied voltage is maximum at 90 degrees so the gate current has to reach minimum gate current value somewhere between zero to 90 degrees.

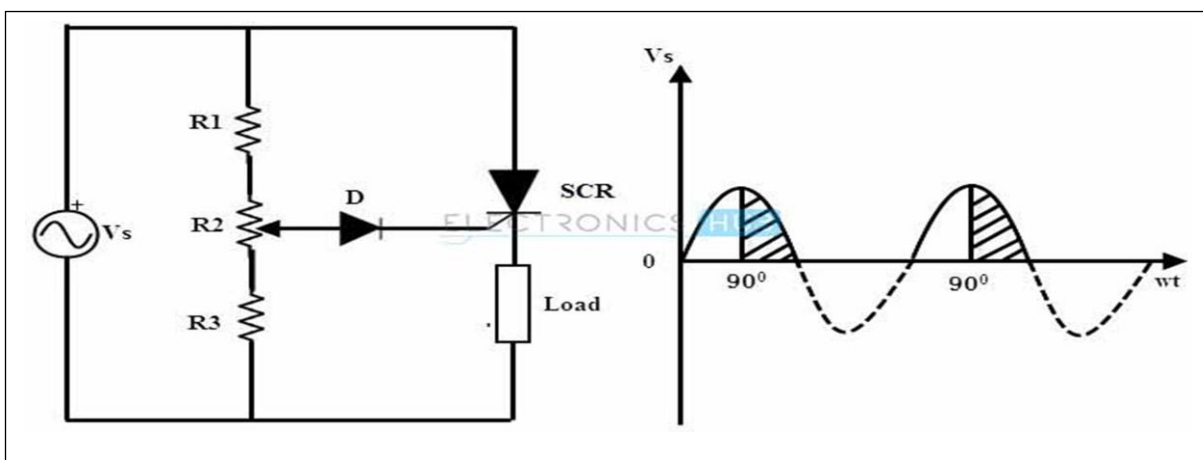


Fig. 1 Rfiring circuit

2- Resistance – Capacitance (RC) Firing Circuit

The limitation of resistance firing circuit can be overcome by the RC triggering circuit which provides the firing angle control from 0 to 180 degrees. By changing the phase and amplitude of the gate current, a large variation of firing angle is obtained using this circuit.

Below fig.2 shows the RC triggering circuit consisting of two diodes with an RC network connected to turn the SCR.

By varying the variable resistance, triggering or firing angle is controlled in a full positive half cycle of the input signal.

During the negative half cycle of the input signal, capacitor charges with lower plate positive through diode D_2 up to the maximum supply voltage. This voltage remains at - across the capacitor till supply voltage attains zero crossing.

During the positive half cycle of the input, the SCR becomes forward biased and the capacitor starts charging through variable resistance to the triggering voltage value of the SCR.

When the capacitor charging voltage is equal to the gate trigger voltage, SCR is turned ON and the capacitor holds a small voltage. Therefore the capacitor voltage is helpful for triggering the SCR even after 90° of the input waveform.

In this, diode D_1 prevents the negative voltage between the gate and cathode during the negative half cycle of the input through diode D_2 .

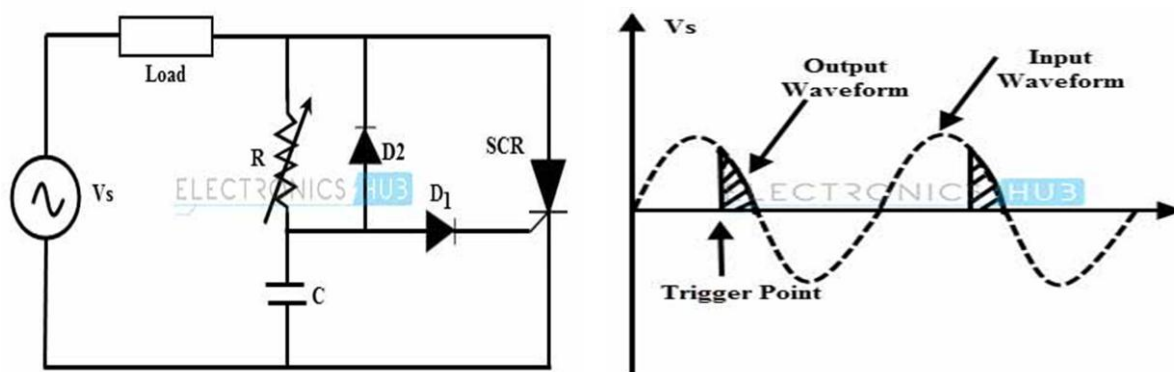


Fig. 2 RC firing circuit

3- UJT Firing Circuit

The Unijunction Transistor (UJT) solid state three terminal device that can be used in gate pulse, timing circuits and trigger generator applications to switch and control either thyristors and triacs for **AC power control type applications**

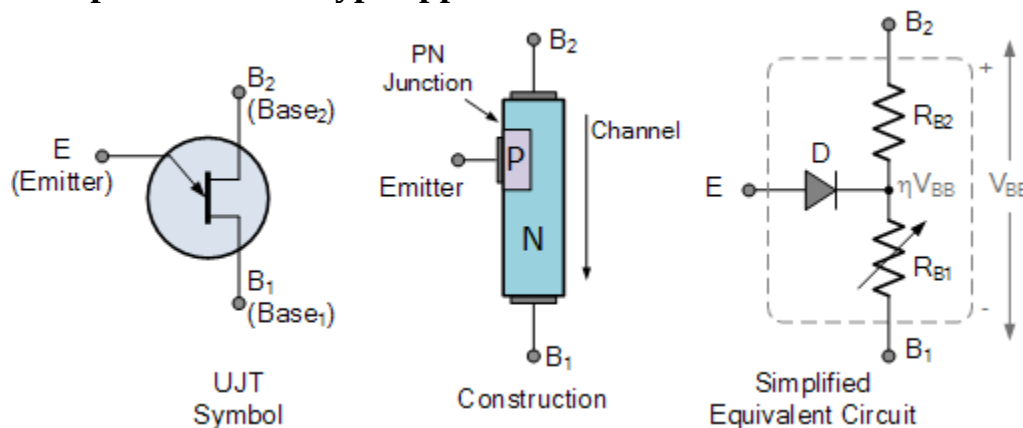


Fig. 3 UJT symbol, construction and equivalent circuit

Uni junction Transistor has the name of a transistor, its switching characteristics are very different from those of a conventional bipolar or field effect transistor as it can't be used to **amplify a signal but instead is used as a ON-OFF switching transistor**.

UJT's have **unidirectional conductivity and negative impedance characteristics** acting more like a variable voltage divider during breakdown.

The UJT consists of a single solid piece of **N-type semiconductor material** forming the main current carrying channel with its two outer connections marked as *Base 2*(B_2) and *Base 1*(B_1). The third terminal marked as the *Emitter*(E) is located along the channel.

The emitter terminal is represented by an arrow pointing from the P-type emitter to the N-type base.

From the equivalent circuit of fig.3 , the N-type channel basically consists of two resistors R_B and R_{B1} in series with an equivalent (ideal) diode, D representing the p-n junction connected to their center point. This Emitter p-n junction is fixed in position along the ohmic channel during manufacture and can therefore not be changed.

Resistance is given between the Emitter, E and terminal , while resistance is given between the Emitter, E and terminal . As the physical position of the p-n junction is closer to terminal B_2 than **the resistive value of R_{B2} will be less than R_{B1}** .

These two series resistances produce a voltage divider network between the two base terminals of the UJT and since this channel stretches from B_2 to , when a voltage is applied across the device, the potential at any point along the channel will be in proportion to its position between terminals B_2 and . The level of the voltage gradient therefore depends upon the amount of supply voltage.

When used in a circuit, terminal is connected to ground and the Emitter serves as the input to the device. Suppose a voltage is applied across the UJT between B_2 and B_1 so that B_2 is biased positive relative to . With zero Emitter input applied, the voltage developed across R_B (the lower resistance) of the resistive voltage divider can be calculated as

Unijunction Transistor R_{B1} Voltage

$$V_{RB1} = \frac{R_{B1}}{R_{B1} + R_{B2}} \times V_{BB}$$

The resistive ratio of R_{B1} to R shown above is called the **intrinsic stand-off ratio** and is given the Greek symbol: η (eta).

$$\eta(\text{eta}) = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

Typical **standard values of η range from 0.5 to 0.8 for most common UJT's**

If a small positive input voltage which is less than the voltage developed across resistance, R_B (ηV_{BB}) is now applied to the Emitter input terminal, the diode p-n junction is reverse biased, thus offering a very high impedance and the device does not conduct. The UJT is switched "OFF" and zero current flows.

However, when the Emitter input voltage is increased and becomes greater than V_{RB1} (or $\eta V_{BB} + 0.7V$, where 0.7V equals the p-n junction diode volt drop) the p-n junction becomes forward biased and the UJT begins to conduct. The result is that Emitter current, ηI_E now flows from the Emitter into the Base region.

The effect of the additional Emitter current flowing into the Base reduces the resistive portion of the channel between the Emitter junction and the B_1 terminal. This reduction in the value of R_B resistance to a very low value means that the Emitter junction becomes even more forward biased resulting in a larger current flow. The effect of this results in a negative resistance at the Emitter terminal.

UJT as SCR firing circuit

The most common application of a UJT is as a **triggering device for SCR and Triac** but other UJT applications include **saw-toothed generators, simple oscillators, phase control, and timing circuits**. The simplest of all UJT circuits is the Relaxation Oscillator producing non-sinusoidal wave forms . In a basic and typical UJT relaxation oscillator circuit, the Emitter terminal of the UJT is connected to the junction of a series connected resistor and capacitor, RC circuit as shown below.

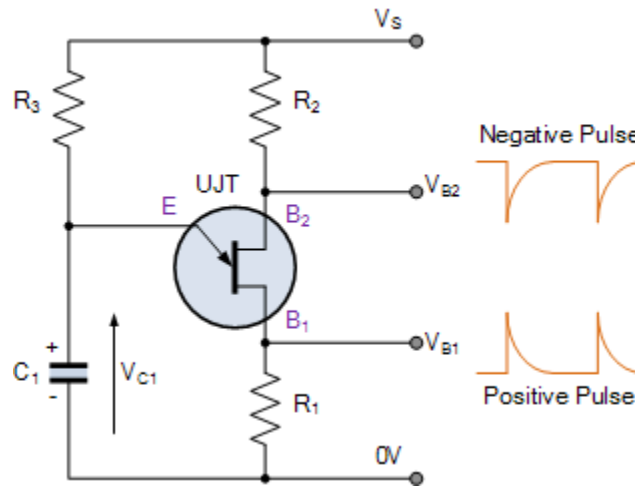


Fig. 4 UJT firing circuit

When a voltage (V_s) is firstly applied, the UJT is “OFF” and the capacitor is fully discharged but begins to charge up exponentially through resistor R_3 . As the Emitter of the UJT is connected to the capacitor, when the charging voltage V across the capacitor becomes greater than the diode volt drop value, the p-n junction behaves as a normal diode and becomes forward biased triggering the UJT into conduction. The UJT is “ON”. At this point the Emitter to B_1 impedance collapses as the Emitter goes into a low impedance saturated state with the flow of Emitter current through R_1 taking place. As the ohmic value of resistor R_1 is very low, the capacitor discharges rapidly through the UJT and a fast rising voltage pulse appears across R_1 . Also, because the capacitor discharges more quickly through the UJT than it does charging up through resistor R_3 , **the discharging time is a lot less than the charging time** as the capacitor discharges through the low resistance UJT. When the voltage across the capacitor decreases below the holding point of the p-n junction (V_{OFF}), the UJT turns “OFF” and no current flows into the Emitter junction so once again the capacitor charges up through resistor R_3 and this charging and discharging process between V_{ON} and V_{OFF} is constantly repeated while there is a supply voltage, V_s applied.

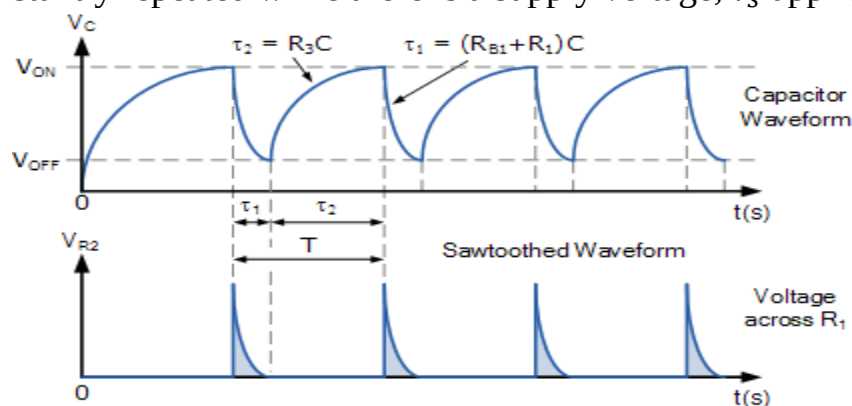


Fig. 5 UJT Oscillator Waveforms

The frequency of operation of the oscillator is directly affected by the value of the charging resistance R_3 , in series with the capacitor C_1 and the value of η . The output pulse shape generated from the Base1 (B_1) terminal is that of a saw tooth wave form and to regulate the time period, you only have to change the ohmic value of resistance, R_3 since it sets the RC time constant for charging the capacitor. The time period, T of the sawtoothed waveform will be given as the charging time plus the discharging time of the capacitor. As the discharge time, τ_1 is generally very short in comparison to the larger RC charging time, τ_2 the time period of oscillation is more or less equivalent to $T \cong \tau_2$. The frequency of oscillation is therefore given by $f = 1/T$.

UJT is the most common method of triggering the SCR because the prolonged pulses at the gate using R and RC triggering methods cause more power dissipation at the gate so by using UJT as triggering device **(the power loss is limited as it produce a train of pulses)**.

The RC network is connected to the emitter terminal of the UJT which forms the timing circuit. The capacitor is fixed while the resistance is variable and hence the charging rate of the capacitor depends on the variable resistance means that the controlling of the RC time constant.

When the voltage is applied, the capacitor starts charging through the variable resistance. By varying the resistance value voltage across the capacitor get varied. Once the capacitor voltage is equal to the peak value of the UJT, it starts conducting and hence produce a pulse output till the voltage across the capacitor equal to the valley voltage of the UJT. This process repeats and produces a train of pulses at base terminal 1.

The pulse output at the base terminal 1 is used to turn ON the SCR at predetermined time intervals.

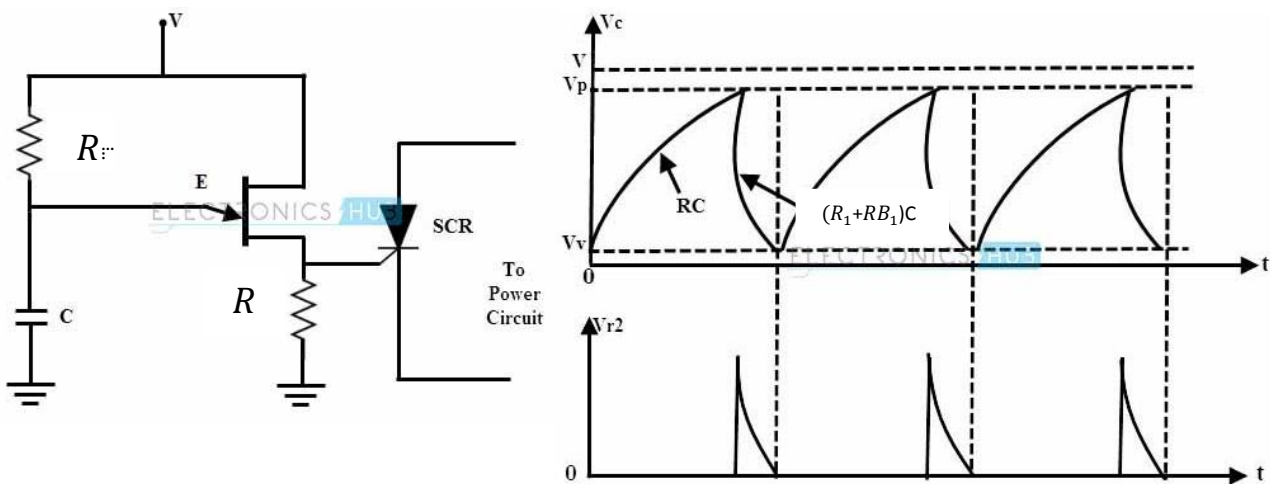


Fig. 6 UJT firing circuit of SCR

Characteristics of UJT

Initially, in the cut-off region, as V_E increases from zero, slight leakage current flows from terminal B_1 to the emitter. This current is due to the minority carriers in the reverse biased diode. Above a certain value of V_E , forward I_E begins to flow, increasing until the peak voltage V_P and current I_P are reached at point P. After the peak point P, an attempt to increase V_E is followed by a sudden increase in emitter current I_E with a corresponding decrease in V_E . This is a negative resistance portion. The negative portion of the curve lasts until the valley point V_V is reached. After the valley point, the device is driven to saturation.

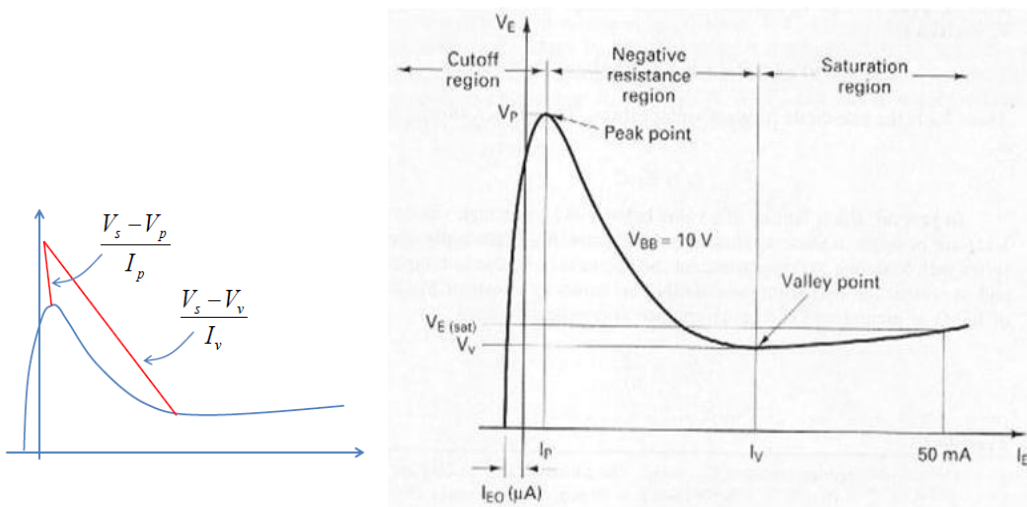


Fig. 1 Characteristics of UJT

Design of UJT

The load line formed by R and C should intersect the device characteristics to the right of peak point but to the left of valley point, otherwise UJT will not turn on.

Therefore min&max values for R

$$\frac{V_s - V_v}{I_v} < R < \frac{V_s - V_P}{I_P}$$

Where V_s can be calculated as

$$V_P = V_1 + V_D = \eta V_{BB} + V_D$$

assume $V_S \cong V_{BB}$

VD: One diode fwd voltage drop, $\approx 0.5V$

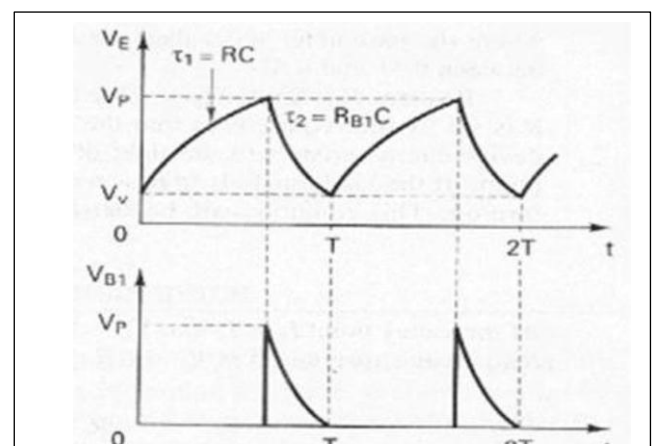
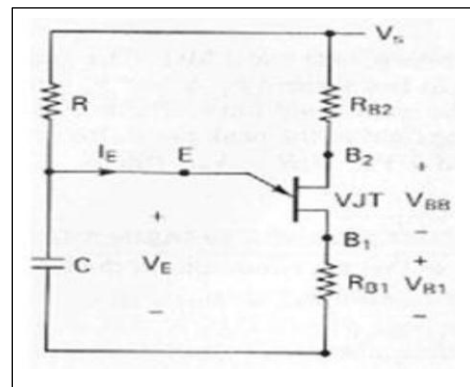
The pulse width of triggering pulse t_g is

$$t_g = R_{B1}C$$

Oscillation frequency is

$$T = \frac{1}{f}$$

A resistor R_{B2} is generally connected in series



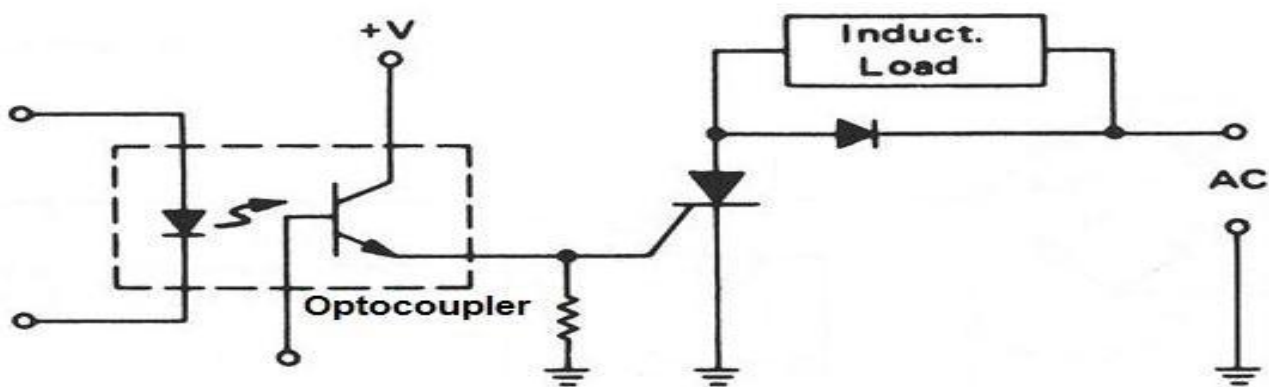
with B_2 to compensate for the decrease in V_p due to temperature rise and to protect the UJT from thermal runaway.

The following points should be considered in designing the gate control circuit;

The gate signal should be removed after the thyristor is turned on. A continuous gate signal increases the power loss in the gate junction.

While thyristor is reversed biased, there should be no gate signal; otherwise, the thyristor may fail due to increased leakage current.

The width of gate pulse t_G must be longer than the time required for the anode current to reach the holding current.



Opto isolated gate drive

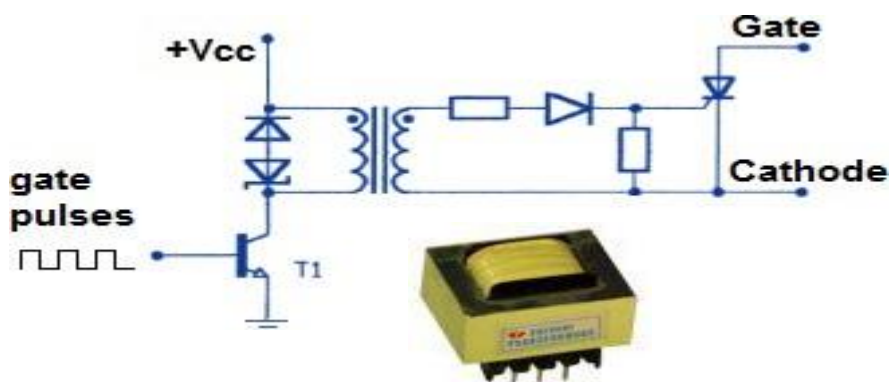


Fig.2 Opto isolated gate drive & Pulse transformer isolated gate drive